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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/009,649	VORBACH ET AL.	
	Examiner	Art Unit	
	Thuy Dao	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *179-181 and 183-203* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *179-181 and 183-203* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date : 06/30/10, 07/22/2010, 08/23/2010, 09/15/2010, and 10/26/2010.

DETAILED ACTION

1. This action is responsive to the Applicant's reply filed on October 5, 2010.

2. Claims 179-181 and 183-203 have been examined.

Response to Amendments

3. The objection to the claims and abstract is withdrawn in view of Applicant's amendments.

Response to Arguments

4. Applicant's arguments have been fully considered.

a) Rejection of Claims 179 and 180:

Examiner notes that Applicant's amendment necessitated the new mappings/ground(s) of rejection presented in this Office action.

b) Rejection of Claims 194-202:

Examiner notes that Applicant's amendment necessitated the new mappings/ground(s) of rejection presented in this Office action.

c) Rejection of Claim 180:

Examiner notes that Applicant's amendment necessitated the new mappings/ground(s) of rejection presented in this Office action.

d) Rejection of Claims 179-181 and 183-189:

Examiner notes that Applicant's amendment necessitated the new mappings/ground(s) of rejection presented in this Office action.

e) Rejection of Claims 190-193:

Examiner notes that Applicant's amendment necessitated the new mappings/ground(s) of rejection presented in this Office action.

f) Rejection of Claim 203:

Examiner notes that Applicant's amendment necessitated the new mappings/ground(s) of rejection presented in this Office action.

Claim Rejections – 35 USC §101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Based upon consideration of all of the relevant factors with respect to the claim as a whole, claims 179-181, 190, 194, and 203 are held to claim an abstract idea, and is/are therefore rejected as ineligible subject matter under 35 U.S.C. 101. The rationale for this finding is explained below: the method claims do not require machine implementation or do not particularly transform a particular article to a different state or thing. The method steps may simply claim an abstract idea or a mental process to perform the above method steps.

Dependent claims when analyzed as a whole are held to be patent ineligible under 35 U.S.C. 101 because the additional recited limitation(s) fail(s) to establish that the claim(s) is/are not directed to an abstract idea.

Under the principles of compact prosecution, the claims have been examined as the Examiner anticipates the claims will be amended to obviate these 35 USC § 101 issues. For example, - -*A method, executed by a central processing unit (CPU), for programming a system*…- -.

Claim Rejections – 35 USC §102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a

> patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 179 and 180 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 5,966,534 to Cooke et al. ("Cooke").

Claim 179:

Cooke discloses *a method for programming a system having a cellular structure of runtime reconfigurable cells, comprising:*

extracting a control flow graph of a program (col.2: 23-37; col.3: 62 – col.4: 26)

to be executed by the cellular structure of runtime reconfigurable cells (FIG.2 and related text, Field Programmable Gate Array FPGA)*;*

separating the control flow graph into a plurality of subgraphs (col.5: 42 – col.6: 34, dividing/partitioning the control flow graph into separate tasks/blocks, wherein each task/block is part of said control flow graph)

such that each of the plurality of subgraphs corresponds to a respective single configuration of each of a respective plurality of the runtime configurable cells (col.3: 35-62; col.5: 31-42)*;*

distributing the plurality of subgraphs among the runtime reconfigurable cells for execution of the subgraphs by the runtime reconfigurable cells (col.6: 38 – col.7: 14, distributing tasks/blocks to FPGA blocks)*;*

determining state information by execution of each of at least a subset of the subgraphs (col.6: 29-34)*; and*

outputting the state information determined by execution of one of the at least the subset of the subgraphs from the one of the at least the subset of the subgraphs (col.6: 1-17 and 38-64) *and*

transferring the state information determined by the execution of the one of the at least the subset of the subgraphs to a subsequently executed subgraph (col.6: 29-34, immediate predecessors are executed (i.e., state information has been sent/received) → successor is (i.e., subsequently executed task/subgraph) now ready and can be inserted into a priority queue)

the state information being used by the subsequently executed subgraphs as a trigger of conditional processing (col.5: 50 – col.6: 18; col.6: 38 - col.7: 31).

Claim 180:

Cooke discloses *a method for programming a system having a cellular structure of runtime reconfigurable cells, comprising:*

extracting a data flow graph of a program (col.2: 23-67; col.3: 63 – col.4: 16)

to be executed by the runtime reconfigurable cellular structure of runtime reconfigurable cells (col.5: 50 – col.6: 18; col.6: 38 - col.7: 31) *and*

that includes a loop (FIG.3 and related text, source code has outer and inner loops)*;*

partitioning the data flow graph, thereby forming a plurality of subgraphs, such that the loop is split into several of the subgraphs (col.3: 63 – col.4: 16; col.6: 1-17 and 38-64)*; and*

such that each of the plurality of subgraphs corresponds to a respective single configuration of each of a respective plurality of the runtime configurable cells (col.6: 38 – col.7: 14, distributing tasks/blocks to FPGA blocks)*; and*

distributing the plurality of subgraphs among the runtime reconfigurable cells for execution of the subgraphs by the runtime reconfigurable cells (col.2: 23-67; col.4: 18—col.5: 41).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 194-202 are rejected under 35 U.S.C. 102(b) as being anticipated Getzinger (by US Patent No. 4,972,314).

Claim 194:

Getzinger discloses *a method of executing a program on an array of runtime reconfigurable cells* (col.14: 31 – col.16: 2)*, the method comprising:*

forming a plurality of subgraphs based on a program (e.g.,

FIG. 1, Graph Process Controller, col.4: 63-67; a plurality of subgraphs as node structures, col.9: 37-48;

node instances (subgraph instances) are ready to "independently and concurrently" executed by placing them on a dispatch queue, col.11: 60-67 and col.1: 52-59;

nodes (subgraphs) are scheduled and dispatched to 16 Arithmetic Processors AP 1-16, col.16: 65 – col.17:21 and FIG. 1)

such that each of the plurality of subgraphs corresponds to a respective single configuration of each of a respective plurality of the runtime configurable cells (col.38: 29 – col.40: 10; col.49: 40 – col.51: 38)*;*

performing, by a first one of the reconfigurable cells, a function corresponding to a first part of a first one of the subgraphs (FIG.12-16, col.18: 23; col.11: 60 - col.12: 29)

while the first cell is configured according to the configuration to which the first subgraph corresponds (col.38: 29 – col.40: 10; col.49: 40 – col.51: 38)*;*

after the computing, reconfiguring the first cell for performing a function corresponding to a first part of a second one of the subgraphs (e.g., col.11: 60 - col.12: 29)*;*

the reconfiguration being to the configuration to which the second subgraph corresponds (e.g., FIG. 1, Parallel Processing Concept with 16 Arithmetic Processors 1-16, col.5: 64 – col.6: 14)*; and*

simultaneously with the reconfiguring, performing, by a second one of the reconfigurable cells (col.38: 29 – col.40: 10; col.46: 5 - col. 47: 26)

a function corresponding to second part of the first subgraph while the second cell is configured according to the configuration to which the first subgraph corresponds (col.38: 29 – col.40: 10; col.49: 40 – col.51: 38)*;*

wherein state information determined for one of the subgraphs is transferred from the one of the subgraphs to a subsequently executed subgraph (e.g., FIG. 5, simultaneously, computing second part C of first subgraph {A, C} with a second Arithmetic Processor AP 2, please see more in FIG. 3 with Dispatch Queue, Arithmetic Processors (in the instant case: 2 APs), Graph Process Controller GPC Scheduler, col.11: 60 - col.12: 29).

Claim 195:

The rejection of base claim 194 is incorporated. Getzinger also discloses *storing configurations for the first one of the subgraphs and the second one of the subgraphs configuration registers associated with the first cell* (col.38: 29 – col.40: 10; col.49: 40 – col.51: 38).

Claim 196:

The rejection of intervening claim 195 is incorporated. Getzinger also discloses *marking unconfigured ones the configuration registers as unconfigured* (FIG.12-16, col.18: 23; col.11: 60 - col.12: 29).

Claim 197:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on a status signal generated by the cell structure* (col.7: 22 – col.8: 29; col.17: 22-59).

Claim 198:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on a status signal generated by a higher-level loading unit* (col.11: 60 – col.12: 30; col.28: 48 – col.29: 36).

Claim 199:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on an externally generated status signal* (col.38: 29 – col.40: 10; col.49: 40 – col.51: 38).

Claim 200:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell as a function of a present configuration of the first cell and a received status signal* (e.g., col.7: 22 – col.8: 29; col.14: 31-66).

Claim 201:

The rejection of base claim 194 is incorporated. Getzinger also discloses:

activating an unconfigured configuration register in the first cell (e.g., col.28: 48 – col.29: 36)*;*

requesting a configuration from a higher-level load unit when the unconfigured configuration register is activated (e.g., col.7: 22 – col.8: 29)*; and*

suspending execution of a subgraph until the requested configuration is fully loaded (e.g., FIG. 7, Graph Process Controller Functions, col.14: 31-66).

Claim 202:

The rejection of base claim 194 is incorporated. Getzinger also discloses *triggering a loading of a configuration of the first cell when a status signal generated by the cell structure received by the first cell* (col.49: 40 – col.51: 38).

Claim Rejections – 35 USC §103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 180 is rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell (US Patent No. 5,021,947) in view of Powell (US Patent No. 5,606).

Claim 180:

Campbell discloses *a method for programming a system having a cellular structure of runtime reconfigurable cells* (col.1: 24 – col.2: 62)*, comprising:*

extracting a data flow graph of a program (col.2: 19 – col.3: 3; col.19: 3 – col.20: 12)

to be executed by the runtime reconfigurable cellular structure of runtime reconfigurable cells (col.9: 3 – col.10: 60; col.17: 1 – col.18: 14) *and*

that includes a loop (col.8: 21-63; FIG.1, blocks 60 and 70; FIG.17, blocks 210-215-220-221)*;*

partitioning the data flow graph, thereby forming a plurality of subgraphs, such that the loop is split into several of the subgraphs (col.3: 53 – col.4: 15; FIG.1, block 60; FIG.17, block 210)*; and*

such that each of the plurality of subgraphs corresponds to a respective single configuration of each of a respective plurality of the runtime configurable cells (FIG.1, block 40 and related text; col.12: 27-63; col.15: 6 – col.16: 36)*; and*

distributing the plurality of subgraphs among the runtime reconfigurable cells for execution of the subgraphs by the runtime reconfigurable cells (col.13: 30 – col.14: 54; col.17: 1-15).

Campbell does not explicitly disclose *the loop is split into several of the subgraphs.*

However, in an analogous art, Powell further discloses *the loop is split into several of the subgraphs* (col.7: 32 – col.8: 45).

12. Claims 179-181 and 183-189 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo (US Patent No. 5,801) in view of Asano (US Patent No. 5,572,710).

Claim 179:

Dangelo discloses *a method for programming a system, comprising:*

extracting a control flow graph of a program to be executed (e.g., col.62: 6-27; col.17: 60 – col.18: 57; col.16: 37-59; col.17: 54-67)*;*

separating the control flow graph into a plurality of subgraphs (e.g., col.62: 6-27; col.17: 60 – col.18: 57; col.16: 37-59; col.17: 54-67; col.31: 1-36; col.54: 49 col.55: 2; col.39: 29-45; col.57: 26-35)

such that each of the plurality of subgraphs corresponds to a respective single configuration of each of a respective plurality of cells (col.27: 60 – col.28: 62; col.34: 51 – col.35: 48)*;*

distributing the plurality of subgraphs among the cells for execution of the subgraphs by the cells (col.33: 46 – col.34: 65; col.62: 6-59)*;*

determining state information by execution of each of at least a subset of the subgraphs (e.g., col.17: 59 – col.18: 37; col.28: 26-54; col.61: 7-34)*; and*

outputting the state information determined by execution of one of the at least the subset of the subgraphs from the one of the at least the subset of the subgraphs (col.61: 7- col.62: 48; col.75: 4 – col.76: 52) *and*

transferring the state information determined by the execution of the one of the at least the subset of the subgraphs to a subsequently executed subgraph (e.g., col.31: 1-36; col.54: 49 col.55: 2; col.39: 29-45; col.57: 26-35)

the state information being used by the subsequently executed subgraphs as a trigger of conditional processing (e.g., col.71: 50 – col.72: 49; col.73: 27-55; col.75: 4-67).

However, in an analogous art, Asano further discloses:

the plurality of programmable hardware modules of the runtime reconfigurable cellular structure (FIG.1, 10, 29, 33 and related text)*; and*

the plurality of subgraphs to be executed by the runtime reconfigurable cellular structure (FIG.22, 32, 33 and related text).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Asano's teaching into Dangelo's teaching. One would have been motivated to do so to utilize a FPGAs as runtime reconfigurable cellular structures as suggested by Asano (col.2: 12 - col.3: 14).

Claim 180:

Dangelo discloses *a method for programming a system, comprising:*

extracting a data flow graph of a program to be executed and that includes a loop (e.g., col.82: 1-42; col.52: 2-44; FIG. 1, ASIC chip 110; col.16: 51-58; col.62: 6-32; col.33: 46-61; FIG. 20b, multi-chip module 2000)*;*

partitioning the data flow graph, thereby forming a plurality of subgraphs, such that the loop is split into several of the subgraphs (FIG.22, 32, 33 and related text)*; and*

such that each of the plurality of subgraphs corresponds to a respective single configuration of each cell (e.g., col.48: 1-40; col.62: 6-27)*; and*

distributing the plurality of subgraphs among the cells for execution of the subgraphs by the cells (e.g., FIG. 25b, col.38: 58-65; col.79: 22-48; FIG. 36g, col.82: 1-32; FIG. 36f, col.81: 52-57).

Dangelo does not disclose *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells.*

However, in an analogous art, Asano further discloses *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells* (FIG.1, 10, 29, 33 and related text).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Asano's teaching into Dangelo's teaching. One would have been motivated to do so to utilize a FPGAs as runtime reconfigurable cellular structures as suggested by Asano (col.2: 12 - col.3: 14).

Claim 181:

The rejection of claim 180 is incorporated.

Dangelo does not disclose *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells.*

However, in an analogous art, Asano further discloses *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells* (FIG.1, 10, 29, 33 and related text).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Asano's teaching into Dangelo's teaching. One would have been motivated to do so to utilize a FPGAs as runtime reconfigurable cellular structures as suggested by Asano (col.2: 12 - col.3: 14).

Claim 183:

Dangelo discloses *the method of claim 181, wherein the separating includes separating the at least one the graphs into the plurality of subgraphs so that data transmission between the plurality of subgraphs is minimized* (e.g., col.75: 42-54; col.78: 16-65; col.80: 3-40).

Claim 184:

Dangelo discloses *the method of claim 181, wherein the separating includes separating the at least one of the graphs into the plurality of subgraphs so that no loop-*

back is obtained between the plurality of subgraphs (col.61: 7- col.62: 48; col.75: 4 – col.76: 52).

Claim 185:

Dangelo discloses *the method of claim 181, wherein the separating includes separating the at least one of the graphs into the plurality of subgraphs so that the subgraphs match resources of the hardware modules* (e.g., col.17: 44-67; col.59: 63 – col.60: 16).

Claim 186:

Dangelo discloses *the method of claim 181, wherein memory elements are inserted between the plurality of subgraphs, the memory elements adapted to save data passed between subgraphs* (e.g., col.62: 48-66; col.71: 1-14; FIG. 25c and related text) (e.g., col.75: 42-54; col.78: 16-65; col.80: 3-40).

Claim 187:

Dangelo discloses *the method of claim 181, wherein each of the plurality of subgraphs includes nodes, the method further comprising: transmitting status signals between nodes within one of the subgraphs so that a state of each individual one of the nodes of the one of the subgraphs is available to each of the other nodes of the one of the subgraphs* (e.g., col.30: 25-49; col.31: 1-30; col.26: 15-32; col.74; 15-24).

Claim 188:

Dangelo discloses *the method of claim 181, wherein each of the plurality of subgraphs includes nodes, the method further comprising: transmitting status signals from a first node of at least one of the plurality of subgraphs to a higher-level unit adapted to control configuration of the plurality of hardware modules so as to trigger reconfiguration* (col.61: 7- col.62: 48; col.75: 4 – col.76: 52).

Claim 189:

Dangelo discloses *the method of claim 181, wherein the extracting includes, for a conditional instruction, extracting a plurality of different subgraphs, each representing a different instruction path, one of the different subgraphs being executed depending on an evaluation of the conditional instruction* (e.g., col.17: 44-67; col.59: 63 – col.60: 16).

13. Claims 190-193 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo in view of McGeer (US Patent No. 6,421,808) and Asano.

Claim 190:

Dangelo discloses *a method of executing a single program on a system, comprising:*

separating the single program into several subgraphs (e.g., col.17: 17-43; col.26: 15-46; col.47: 50-67; col.52: 15-39)

such that each of the subgraphs corresponds to a respective single configuration (e.g., col.31: 1-36; col.54: 49 col.55: 2; col.39: 29-45; col.57: 26-35)*;*

distributing the several subgraphs (e.g., col.17: 54 – col.18: 37; col.21: 45-67)*; and*

executing the several subgraphs (col.33: 46 – col.34: 65; col.62: 6-59),

the executing including: transmitting a data signal from a first cell via which a first one of the subgraphs is executed to a second cell via which a second one of the subgraphs is executed (col.61: 7- col.62: 48; col.75: 4 – col.76: 52).

Dangelo does not explicitly disclose *transmitting a status with the data signal, the status indicating whether the data signal is valid.*

However, in an analogous art, McGeer further discloses *transmitting a status with the data signal, the status indicating whether the data signal is valid* (e.g., col.13: 59-67; col.14: 64 – col. 15: 12; col.30: 66 – col.31: 16; col.31: 44-67).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer‘s teaching into Dangelo‘s teaching. One

would have been motivated to do so to perform computation based on valid input signals as suggested by McGeer (e.g., col.3: 26-57).

Dangelo does not disclose *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells.*

However, in an analogous art, Asano further discloses *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells* (FIG.1, 10, 29, 33 and related text).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Asano's teaching into Dangelo's teaching. One would have been motivated to do so to utilize a FPGAs as runtime reconfigurable cellular structures as suggested by Asano (col.2: 12 - col.3: 14).

Claim 191:

McGeer discloses *the method of claim 190, further comprising: receiving a valid data signal at the second cell; and acknowledging receipt of the valid data signal* (e.g., col.15: 43 – col.16: 59).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer's teaching into Dangelo's teaching. One would have been motivated to do so to as set forth above.

Claim 192:

Dangelo discloses *the method of claim 191, further comprising, transmitting by the second cell an indication that a signal is expected* (e.g., col.16: 9-16; col.19: 50 – col.20: 57).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer's teaching into Dangelo's teaching. One would have been motivated to do so to as set forth above.

Claim 193:

Dangelo discloses *the method of claim 192, further comprising: transmitting by the first cell an indication that the first cell is transmitting the expected signal* (e.g., col.15: 43 – col.16: 59; col.16: 9-16; col.19: 50 – col.20: 57).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer's teaching into Dangelo's teaching. One would have been motivated to do so to as set forth above.

14. Claim 203 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo in view of Phillips (US Patent No. 6,708,325) and Asano.

Claim 203:

The rejection of claims 180 and 190 is incorporated. Dangelo does not explicitly disclose other limitations. However, in an analogous art, Phillips further discloses:

extracting a plurality of different subgraphs, each representing a different instruction path of the conditional instruction (e.g., col.6: 23-67),

the conditional instruction indicating which of the executed instruction paths is to be selected for providing output of the selected instruction path output to a further subgraph (e.g., col.3: 66 – col.4: 35; col.7: 47 – col.8: 19)*;*

for each one of the different subgraphs, the system sets execution of the subgraph to be bypassed as soon as an evaluation in accordance with the conditional instruction reveals that output of the subgraph will not be selected (e.g., col.8: 9-19).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Phillips' teaching into Dangelo's teaching. One would have been motivated to do so to perform branch prediction and to load the actually needed configuration in the case of missed prediction as suggested by Phillips (e.g., col.8: 9-19).

Dangelo does not disclose *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells.*

However, in an analogous art, Asano further discloses *a cellular structure of runtime reconfigurable cells and the plurality of subgraphs to be executed by the cellular structure of runtime reconfigurable cells* (FIG.1, 10, 29, 33 and related text).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Asano's teaching into Dangelo's teaching. One would have been motivated to do so to utilize a FPGAs as runtime reconfigurable cellular structures as suggested by Asano (col.2: 12 - col.3: 14).

Conclusion

15. Any inquiry concerning this communication should be directed to examiner Thuy (Twee) Dao, whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570, respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thuy Dao/ (Twee)
Examiner, Art Unit 2192